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A pipelined simulation approach for logic emulation using multi-FPGA platforms

Baviskar, O.; Patkar, S.;
Circuits and Systems, 2009. ISCAS 2009. IEEE International Symposium on
Digital Object Identifier: 10.1109/ISCAS.2009.5117962
Publication Year: 2009 , Page(s): 1141 - 1144

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Static scheduling of multidomain circuits for fast functional verification

Kudlugi, M.; Tessier, R.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on
Volume: 21 , issue: 11
Digital Object Identifier: 10.1109/TCAD.2002.804086
Publication Year: 2002 , Page(s): 1253 - 1268

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